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Design of 125-Level Asymmetrical Multilevel Inverter with Reduced Switch Count

N V Vinay Kumar, T Gowri Manohar

Abstract*: This paper provides a unique reduced component-count-efficient topology for 125-level asymmetrical multilevel inverter. The proposed design uses asymmetric DC sources and an H-bridge to produce an output voltage that can reach a maximum of 125 levels. The design and development of a multi-level inverter with a stacked half-bridge architecture that generates a 125-level output with excellent power quality is the object of the current research. The MOSFETs are triggered using a fundamental frequency switching technique that has been modified for output voltage level control. At its output, the level production circuit exclusively generates positive levels. Look-up tables are employed to regulate MOSFETs, and an H-bridge circuit is used to create polarities. 125 levels of output result in a nearly sinusoidal voltage waveform, which will give a nearly sinusoidal voltage waveform without the use of filters. The proposed work is Simulated in MATLAB/Simulink software.

Keywords: Multilevel Inverter, Pulse width Modulation Technique, Total Harmonic Distortion.

I. INTRODUCTION

Multilevel inverters have recently attracted attention due to their substantial power operation capacity and a number of advantages, including reduced harmonics, decreased electromagnetic interference, high power quality, and fewer switching losses [1]. Employing a power electronic circuitry made up of multiple power semiconductor switches, these MLIs produce a stepped voltage waveform at their output using a variety of DC sources [2]. The level can be expanded to further enhance waveform quality. However, because there are extra devices in the circuit, which results in a higher cost, ensuring the reliability, as well as the performance of MLI, is a difficult task [3]. There are three main types of MLIs: flying capacitors (FC), cascaded H-bridges (CHB), and diodes clamped or neutral point clamped (NPC) [4]. Single DC source and Multi DC source are the names of the CHBMLI. The CHBMLI are parallelly coupled in a single DC source. The CHB multilevel inverters for multi-DC sources use an arrangement of H-Bridge cells with separate DC voltage sources connected to each cell.

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*Correspondence Author(s)
N V Vinay Kumar*, Department of Electrical & Electronics Engineering, Sri Venkateswara University College of Engineering, Sri Venkateswara University, Tirupati, India. Email: vinaynanda.svu@gmail.com, ORCID ID:0000-0002-6266-9928
T Gowri Manohar, Department of Electrical & Electronics Engineering, Sri Venkateswara University College of Engineering, Sri Venkateswara University, Tirupati, India. Email: gowrimanohart@gmail.com, ORCID ID: 0000-0003-0441-6022

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Bipolar and unipolar multilevel converters, which can generate levels naturally or using an H-bridge, are the two main types available. MLIs can provide output voltage values that are both positive and negative. Some additional multilevel converters produce just positive polarity in the first stage, and in the second stage, an H-bridge changes the polarity waveform to bipolar, producing AC voltage as a positive and negative half-cycle. On the other hand, the H-bridge refers to the "polarity-generation part" while the first component, refers to the "level-generation part." H-bridge topologies may have fewer components, but it's possible that H-bridge circuits can withstand a lot of switch stress. The level-generation portion of the suggested architecture in [5] [12] [13] can be built by connecting sub modules in series. H-bridge is inserted as the polarity-generation component at the conclusion of the series connection. Each switch in the level-generation section should withstand the voltage of the relevant DC source(s).

Based on the magnitudes of the DC voltage, the CHB inverter is divided into symmetric and asymmetric types using a variety of single-phase H-bridge topologies. All DC voltage sources in a symmetric MLI are of identical magnitude, in contrast to an asymmetrical MLI where the magnitudes are not. For the same amounts of output voltage, asymmetrical topologies required fewer switching devices and voltage sources than symmetrical topologies. In contrast to typical topologies, the topology described in this paper for a 125-Level Asymmetrical Multilevel Inverter required fewer switching devices

II. MULTILEVEL DC LINK INVERTER TOPOLOGY

The multilayer DC link inverter (MLDCL) is one of the most popular reduced switches MLI topologies, as suggested in (NV, V. K, 2023) [6]. It is an independent type MLI, and separate DC sources are needed depending on the quantity of output levels (R. Agrawal and S. Jain, 2017) [7] [14] [15] [16]. For the same amounts of output voltage, asymmetrical topologies required fewer switching devices and voltage sources than symmetrical topologies. The MLI configuration, shown in Fig.2, consists of an H-bridge inverter circuit called the Polarity generation circuit and an asymmetric basic circuit called the Level generator unit. Compared to a level generation unit, the switches in the polarity generation circuit will be under more stress. MLDCL is a hybrid version of MLI that consists of a stage for level generation and a stage for polarity generation. The circuit block diagram for the 125-level inverter output is shown in Fig.2, where the Level Generation Circuit and Polarity Generation Circuit are both controlled by the Driving Circuit's control signals.

When compared to their symmetric equivalents, asymmetric structures are capable of producing higher levels of output for comparable numbers of semiconductor devices and voltage sources.

The MLDCL inverter topology, which consists of six DC sources, is shown in Figure 2. The level generating stage creates positive and zero voltage levels in the form of a stair-step waveform. In contrast, the H-Bridge-based polarity generating stage alternately inverts each second half-cycle of the waveform formed by the level creation stage into negative levels, providing an output that resembles a sine wave (Venkataramanaiah, Y. Suresh, and A. K. Panda, 2017) [8]. Based on an asymmetrical DC source arrangement, 125 levels of output voltage are produced using the same topology as in Fig. 2. By applying the binary technique, the DC sources are identified for 125 output levels using geometric progression as follows. (N. V. Vinay Kumar and Tenepalli Gowri Manohar, 2024) [9].

$$V6=2V5=2V4 = 2V3 = 2V2 = 2V$$

In contrast to the symmetrical structure, it is possible to generalize the number of levels and switch needed in an asymmetrical MLDCL inverter as follows (M. D. Siddique et al.,2019) [10].

$$N_{L,asym} = 2n + 1 \text{ , } N_{S,asym} = 2n + 4$$

This topology is based on a full bridge cascaded H-bridge inverter and one-stage sub-multilevel converter units connected in series. The power semiconductor switches of the ASCHBMLI are managed by a low-frequency pulse width modulation method. Instead of the many benefits of MLIs, reliability problems are a major concern because more components are needed to reduce THD. To boost reliability while reducing THD, researchers face a crucial problem.

This paper's major goal is to employ fewer switches while adding more levels to the output voltage. In comparison to standard topologies, the suggested topology provides high power capability with lower total harmonic distortion (THD), commutation losses, and the number of switching devices and voltage sources.

This paper presents a new topology based on asymmetrical multilevel inverter (ASMLI), shown in Fig. 2. It required six unequal voltage sources (V1, V2, V3, V4, V5 and V6) and twelve unidirectional switches (S1, S2, S3, S4....S12), which is a combination of IGBT with antiparallel diode to produce the 125-Level single phase output voltage that is found in nature. Due to the unidirectional nature of every semiconductor switching component employed in this circuit, the number of MOSFETs and driver circuits stays constant. The variables that affect switching losses in a multilayer inverter circuit are current, blocking voltage, and switching frequency. The condition of each switch in the level generation unit is shown in Table 1. S1, S2, S3, S4….S12 of the level generating unit, along with T1, and T2 of the polarity generation unit, can be used to create a total of 125 levels. S1, S2, S3, S4…..S12 can all be turned off to achieve zero level. Since the negative half cycle will be in symmetry with the positive cycle, it can be produced by combining T3 and T4 of the polarity production unit with S1, S2, S3, S4…..S12 of the level generation unit.

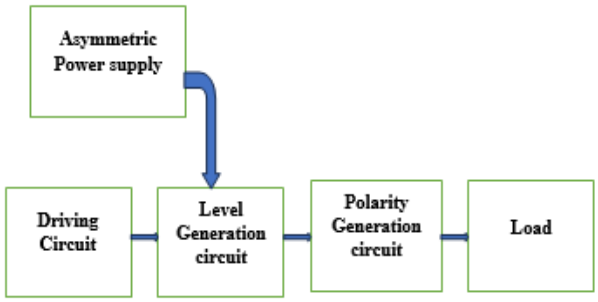

Fig: 1 Control Block Diagram

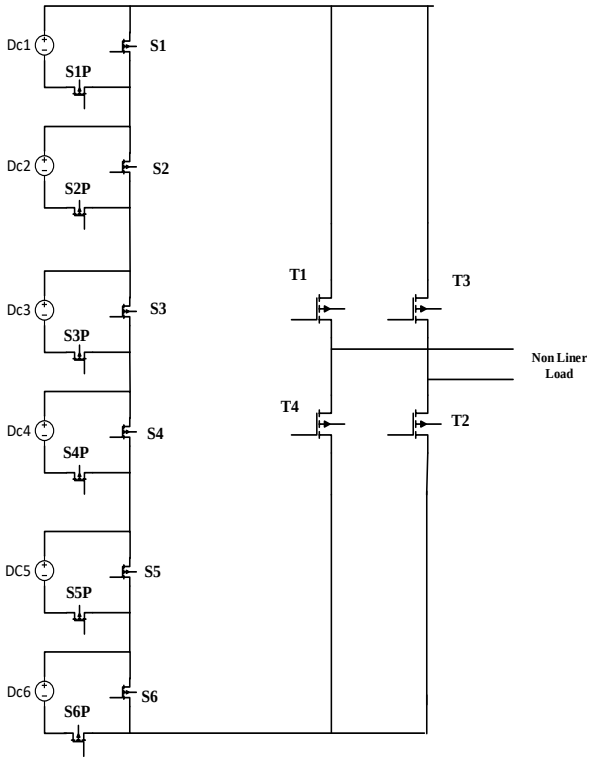

Fig: 2 Proposed 125 level MLDCL Inverter

III. APPROCH FOR PULSE WIDTH MODULATION

In a multilayer inverter (MLI), modulation techniques are employed to create a train of switching pulses that create sinusoidal waveforms at the output voltage. Reference signal and carrier signal are contrasted in modulation techniques [11]. It is necessary to use carrier waves for N-Level inverters (N-1). The MLDCL inverter design does not necessitate the use of a specific modulation approach, with the exception that there may be some variation in the combos of carrier signals that must be compared with the reference signal when generating switching pulses using relational operators. The carrier-based PWM approach is the most popular sort of PWM that may be employed. Every time the

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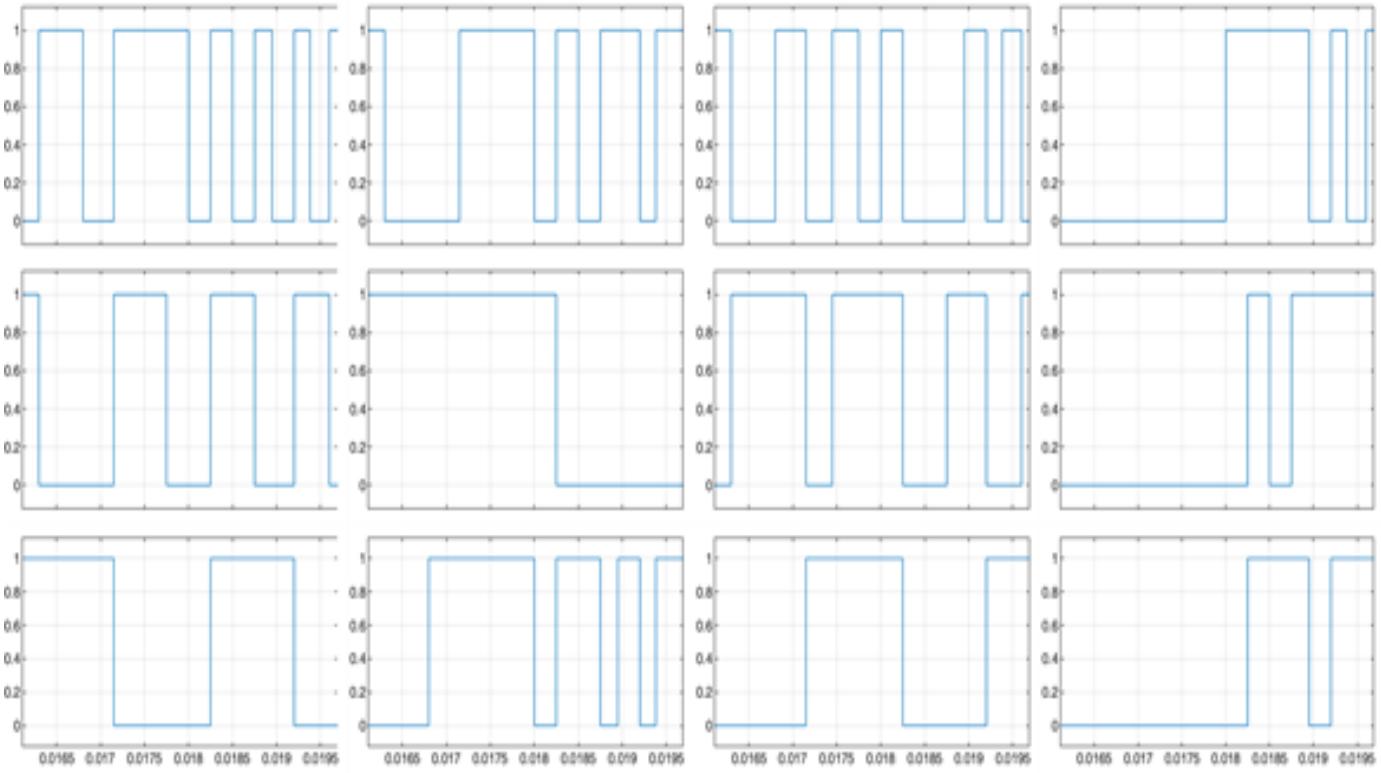

Fig:4 Triggering Pulses for Level Generation

carrier signal is compared to the reference signal, which must always be stronger, the switching pulse displays "1," otherwise it displays "0." The switching pulse is created by adding the comparison results between the reference signal and carrier signal, and the voltage levels are then produced.

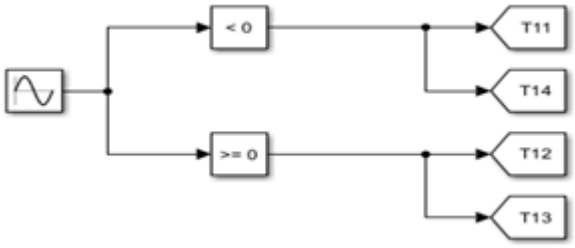

Fig:5 Triggering Pulses for Polarity Generation

IV. SIMULATION RESULTS

Below is an analysis of the 125-level inverter's results with the ideal number of switches. the following list of input voltage sources is used: V1=3.8v, V2=7.6v, V3=15.2v, V4=30.4v, V5=60.8v, V6=121.6v. The output voltage is supposed to have a 50Hz frequency.

TABLE III. Comparison of Required Components between Proposed and Conventional Topologies for 125-level MLI

MLI Components	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Proposed Topology
Switching Devices	248	248	248	**16**
Clamping Diodes	15252	-	-	-
DC Split Capacitor	123	123	-	-
Clamping Capacitors	0	7626	-	-
DC Sources	1	1	62	-
Total	15624	7998	310	**16**

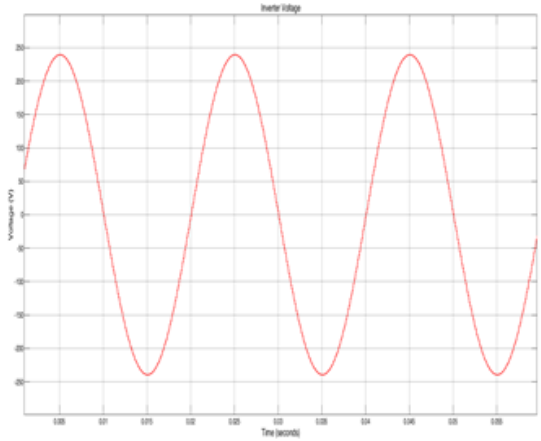

Fig:6 Simulation Result for 125 Level Output

The semiconductor switching MOSFET is provided the output of the pulse generator. These pulses are 1V in magnitude. The harmonic of inverter output voltage is 0.01% which is within the tolerance limit specified by the IEEE standard for harmonics (IEEE 519). Fig. 7 depict this. The 125-level output for the proposed inverter is shown in Figure 6. Simulation is performed for the proposed circuit with MATLAB/SIMULINK.

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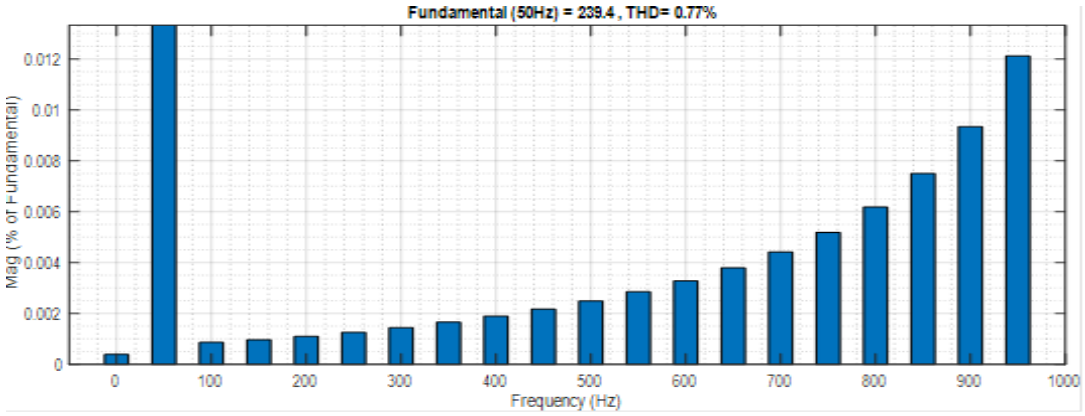

Fig:7 Harmonic Spectrum of 125 level Output

V. CONCLUSION

The paper deals with A 125-Level Asymmetrical Cascaded Multilevel inverter. The Pulse width modulation technique is used for controlling the MOSFET switches. This paper proposes a medium voltage system-optimized multilayered inverter architecture. The main benefit of this design is its simplicity, which allows for a reduction in both the complexity of the driving circuit and the size of the multilayer inverter. The MATLAB/SIMULINK platform is used for simulation. The output is 125 levels with a THD of 0.01%. Additionally, the outcomes can be used to deduce the characteristics of this topology for increasing output levels. The recommended asymmetric topology has been compared to other topologies in terms of the key characteristics. As can be observed, the MLDCL asymmetric structure inverter has lower blocking voltage values for semiconductor switching devices than other topologies that employ asymmetric structures. Simulated outcome for the suggested methods is presented. It has been demonstrated that an inverter with the proposed topology requires fewer MOSFETs. We may reduce the number of gate drivers by employing this topology, which will also result in a smaller circuit.

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I/We hereby declare that this submission is entirely my work, in my own words, and that all sources used in researching it are fully acknowledged and all quotations properly identified.

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Availability of Data and Material	Not relevant.
Authors Contributions	Conceptualization was done by N V Vinay Kumar (NVVK) and T Gowri Manohar (TGM); validation was done by NVVK and TGM; formal analysis was done by NVVK; investigation was done by NVVK; resources were done by NVVK; data curation was done by NVVK; writing—original draft preparation were done by NVVK; writing—review and editing were done by TGM; supervision was done by TGM. NVVK and TGM participated in its design and coordination and helped to draft the manuscript. Both authors have read and agreed to the published version of the manuscript and approved the final manuscript

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AUTHORS PROFILE

N V Vinay Kumar (Corresponding Author) was born in Anantapur city, Andhra Pradesh, India. He received his B.Tech. & M. Tech degree from JNTUA in 2009 & 2012. Currently he is a research scholar in department of Electrical and Electronics Engineering in Sri Venkateswara University college of Engineering, Sri Venkateswara University, Tirupathi, His research interests include Power Converters, Power quality and Optimization Techniques.

Prof. T GowriManohar (Co-Author) was born in Tirupathi City, Andhra Pradesh, India. He is a professor in Dept. of Electrical & Electronics Engg, S.V. University College of Engineering, Sri Venkateswara University, Tirupathi, Andhra Pradesh, India. His research interests include Power System Operation and Control, Power quality and Power Converters.

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